REMARKS

Claims 2-30 are pending in the present application. Claims 9 and 15-30 have been rejected, with all other claims having been indicated as being allowable. Consideration of these remarks and allowance of the claims is respectfully requested.

Applicant wishes to thank the Examiner for allowing claims 2-8 and indicating the allowable subject matter of claims 10-14.

Claims 9 and 15-30 have been rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi (U.S. Patent No. 5,748,024). Applicant respectfully traverses this rejection.

Claim 9 specifically recites:

(1) a second n-channel transistor "coupled to a second voltage level reference node";

(2) an "input signal varying between a first voltage level and a second voltage level";

(3) a second p-channel transistor "coupled to a third reference node"; and

(4) "the third voltage level being different than the first voltage level."

Comparing claim 9 to the Takahashi reference:

(1) Transistor 24 is coupled to ground. For anticipation, therefore, the "second voltage reference node" must be ground.

(2) Takahashi teaches that the input signal 31 of Figure 4 varies between ground and the voltage level VDD. *See* Figure 1a; Figure 4; col. 4, lines 25-30; col. 4, lines 57-59; col. 3, lines 59-60 (and also Applicant's amendment of May 2003). For anticipation, ground and VDD must be the "first voltage level" and the "second voltage level." Moreover, in view of (1) above, the "first voltage" must be VDD, since the "second voltage" is ground.

(3) Transistor 21 is coupled to VDD. For anticipation, therefore, the "third reference node" must be VDD.

(4) Looking at the requirements of (2) and (3) above, the first voltage level (VDD) is not

different than the third voltage level (VDD). Therefore, Takahashi cannot anticipate claim 9.

Claims 10-19 depend from claim 9 and add further limitations. It is respectfully submitted that each of these claims is allowable for reason of depending from an allowable claim as well for adding further limitation.

Claim 20 specifically recites "an enable/disable section including a first portion coupled between the level shifting section and the first voltage node and a second portion coupled between the level shifting section and third reference voltage node." It is respectfully submitted that the reference of record does not teach or suggest the limitations of claim 20.

In the final rejection dated 7/25/2003, the Examiner states on page 4, lines 4-5 that the third voltage level is "VDD less the voltage drop across transistors 21 and 22." But on line 9 of the same page, the Examiner cites to "a third reference voltage node VDD carrying a the third voltage level VDD." However, the third voltage level cannot be both VDD and VDD less a voltage drop. Therefore, Takahashi cannot anticipate claim 22.

Claims 21-30 depend from claim 20 and add further limitations. It is respectfully submitted that each of these claims is allowable for reason of depending from an allowable claim as well for adding further limitation.

In view of the above, Applicant respectfully submits that the formal issues have been resolved. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's agent at the below listed telephone number and address.

Respectfully submitted,

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